INTRODUCTION TO COMPUTER TECHNOLOGIES
Arithmetic Circuits PRETEST

1) The most significant bit of the binary number 100000 is _____.

2) What is the sum of the binary numbers 1111 and 0011? _____

3) What is the difference between the binary numbers 1110110 and 1010? _____

4) The binary numbers 1110110 equals _____ in decimal?

5) A half-adder contains a(n) _____ and a(n) _____ gate.

6) A full-adder contains two _____ circuits.

7) A full-adder has _____ inputs and _____ outputs.

8) A 4-bit parallel adder requires _____.

9) _____ additional _____ gate(s) are required to convert a half-adder into a half-subtractor.

10) Full-adder and Full-subtractor are classified as _____ circuits.

Refer to Fig. 1 (below) for questions 11 - 16.

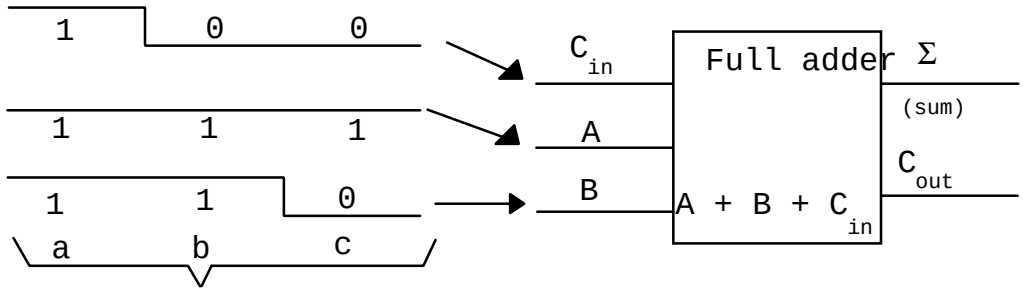

Figure 1

11) The sum output from the full-adder circuit for problem a will be _____ (1 bit).

12) The C_o output from the full-adder circuit for problem a will be _____ (1 bit).

13) The sum output from the full-adder circuit for problem b will be _____ (1 bit).

14) The C_o output from the full-adder circuit for problem b will be _____ (1 bit).

15) The sum output from the full-adder circuit for problem c will be _____ (1 bit).

16) The C_o output from the full-adder circuit for problem c will be _____ (1 bit).

Refer to Fig. 2 (below) for questions 17 - 25.

Figure 2

17) When this unit is adding 1001 to 0101, the control must be _____.

18) When this unit is adding 1001 to 0101, the output sum appears as binary _____ (4 bits).

19) When this unit is adding 1001 to 0101, the C_{in} input to the full-adder is _____ owing to the disabled AND gate

20) The XOR gates function as _____ gates when the control is high (unit in subtract mode).

21) When this unit is in subtract mode, the _____ end-around carry technique is used to allow the adders to perform binary subtraction.

22) When this unit is subtracting 1010 from 1100, the bits appearing at the B inputs to the full adders will be _____ [4 bits , with the 8s bit on the left and the 1s bit on the right].

23) When this unit is subtracting 1010 from 1100, the difference appearing at the output will be binary _____ [4 bits].

24) When this unit is subtracting 1010 from 1100, the end-around carry line will be _____ (HIGH, LOW).

25) This unit can be best described as a(n) _____ adder/subtractor.

26) What is the binary product of 1010 X 0111?

27) What is the binary product of 1111 X 0101?

28) What is the product of 1101_2 X 2_{10} (in binary)?

29) What is the product of 1010_2 X 3_{10} (in binary)?

30) The 1s complement number 0101 represents _____ in decimal.

31) The 1s complement number 1011 represents _____ in decimal.

32) The decimal 13 equals _____ (4 bits) in 1s complement.

33) The decimal 3 equals _____ (4 bits) in 1s complement.

34) When microprocessors process both positive and negative numbers, _____ representation are used.

35) The 2s complement number 0101 represents a positive _____ in decimal.

36) The 2s complement number 1111 represents a negative _____ in decimal.

37) In 2s complement, the MSB is called the _____ bit.

38) The decimal -3 equals _____ (4 bits) in 2s complement.

39) The decimal 6 equals _____ (4 bits) in 2s complement.

40) The decimal -2 equals _____ (4 bits) in 2s complement.

41) The sum of the 2s complement numbers 1011 & 1110 equals _____ (4 bits) in 2s complement.

42) Subtract 2s complement numbers 0011 from 2s complement numbers 1011 (Give answer in 2s complement).

43) Subtract 2s complement numbers 0011 from 2s complement numbers 0111 (Give answer in 2s complement).

44) A five bit adder requires _____ half adder(s) and _____ full adder(s).

45) A seven bit subtractor requires _____ half subtractor(s) and _____ full subtractor(s).

46) A five bit parallel adder/subtractor requires _____ half adder(s), _____ full adder(s), _____ half subtractor(s) and _____ full subtractor(s).