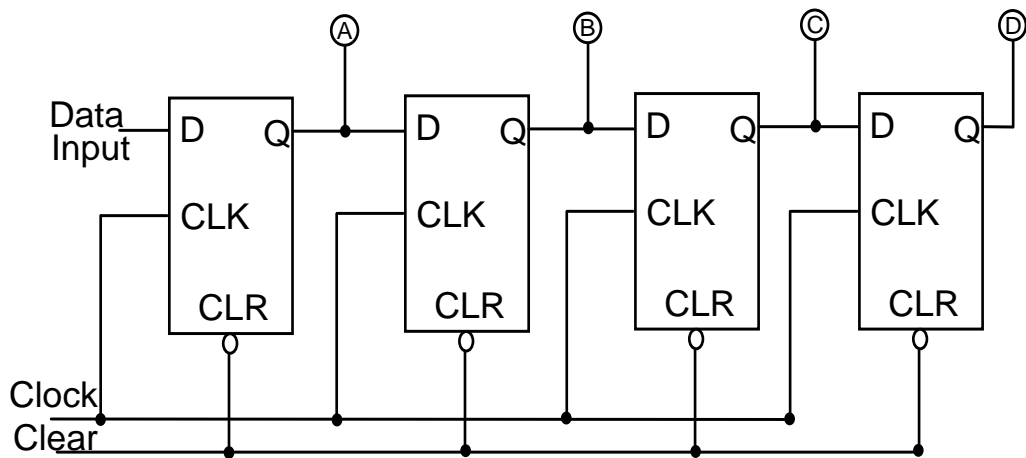


ICT Shift Register HW #1

Line Number	Inputs			Outputs			
	Clear	A	Clock Pulse	FF A	FF B	FF C	FF D
				A	B	C	D
1	0	1					
2	1	1	↗				
3	1	0	↗				
4	1	1	↗				
5	1	1	↗				
6	1	0	↗				
7	1	1	↗				
8	1	0	↗				
9	0	0					
10	1	0	↗				
11	1	1	↗				
12	1	1	↗				
13	1	0	↗				
14	1	1	↗				
15	1	1	↗				
16	1	1	↗				
17	1	0	↗				
18	0	1	↗				

Use the Shift Register Below to fill in the table above:



Line Number	Inputs			Outputs			
	Clear	A	Clock Pulse	FF A	FF B	FF C	FF D
				A	B	C	D
1	0		↗				
2	1	1	↗				
3	1	0	↗				
4	1	1	↗				
5	1	1	↗				
6	0	1	↗				
7	1	0	↗				
8	1	1	↗				
9	1	1	↗				
10	1	0	↗				
11	1	1	↗				
12	1	0	↗				
13	1	0	↗				
14	0	1	↗				
15	0	0	↗				
16	1	1	↗				
17	1	0	↗				
18	0	0	↗				

Use the Shift Register Below to fill in the table above:

