

ICT Shift Register HW #3

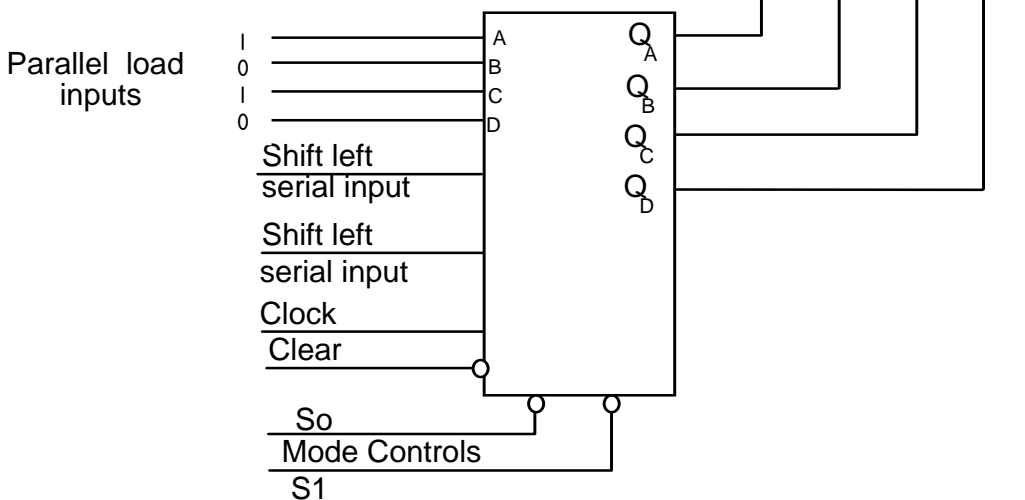
Complete the given table

Line Number	Clear	Shift Left	Shift Right	So	S ₁	Clock Pulse	Outputs			
							A	B	C	D
1	0	x	x			↗				
2		0			0	↗				
3			0		0	↗				
4					0	↗				
5		0	0		0	↗				
6		0			0	↗				
7	0	x	x	x	x	↗				
8		0	0			↗				
9		0	0	0		↗				
10			0	0		↗				
11		0		0		↗				
12	0		0			↗				
13						↗				
14			0		0	↗				
15		0			0	↗				
16		0		0		↗				

Use the Shift Register below to fill in the above table:

Mode Control

Parallel load	So = 1 S ₁ = 1
Shift Right	So = 1 S ₁ = 0
Shift Left	So = 0 S ₁ = 1
Inhibit	So = 0 S ₁ = 0



Complete the given table

Line Number	Clear	Shift Left	Shift Right	So	S1	Clock Pulse	Outputs			
							A	B	C	D
1	0	x	x			↗				
2			0		0	↗				
3		0			0	↗				
4			0		0	↗				
5			0	0		↗				
6		0		0		↗				
7			0	0		↗				
8		0		0		↗				
9						↗				
10		0	0		0	↗				
11				0		↗				
12	0					↗				
13				0		↗				
14		0			0	↗				
15			0	0		↗				
16		0		0		↗				

Use the Shift Register below to fill in the above table:

Mode Control

Parallel load	So = 1 S1 = 1
Shift Right	So = 1 S1 = 0
Shift Left	So = 0 S1 = 1
Inhibit	So = 0 S1 = 0

