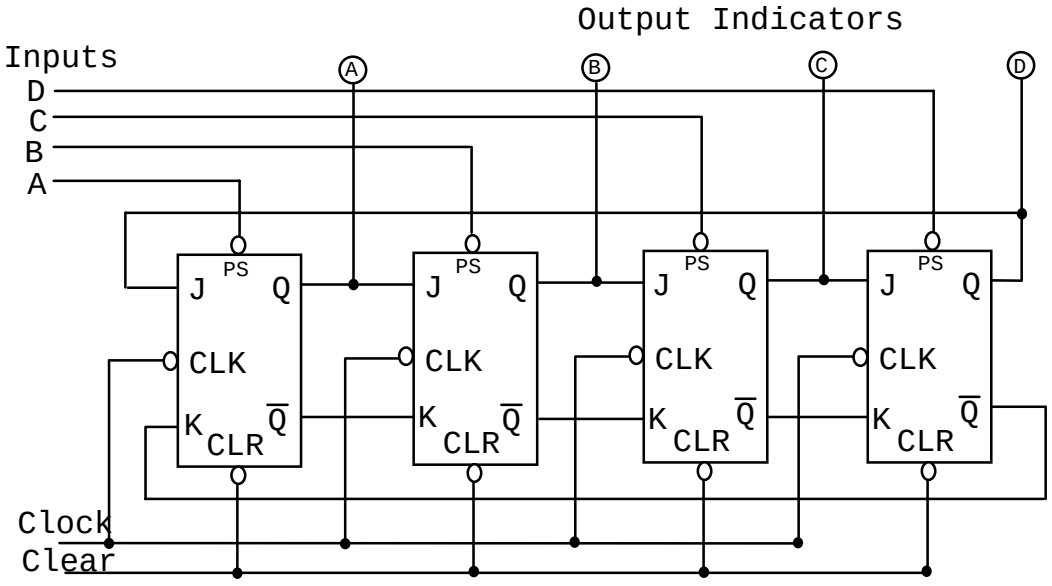
In-Class Parallel Load Shift Register Examples

Inputs							Outputs			
Line Number	Clear	Parallel Load Data				Clock Pulse	FF A	FF B	FF C	FF D
		A	B	C	D		A	B	C	D
1	0	1	1	1	1					
2	1	0	1	0	1					
3	1	1	1	1	1	↑				
4	1	1	1	1	1	↑				
5	1	1	1	1	1	↑				
6	0	1	1	1	1					
7	1	0	0	1	1					
8	1	1	1	1	1	↑				
9	1	1	1	1	1	↑				
10	1	1	1	1	1	↑				
11	1	1	1	0	1					
12	1	1	1	1	1	↑				
13	1	1	1	1	1	↑				
14	0	1	1	1	1					
15	1	0	1	1	0					
16	1	1	1	1	1	↑				
17	1	1	0	0	1					
18	1	1	1	1	1	↑				



Inputs							Outputs			
Line Number	Clear	Parallel Load Data				Clock Pulse	FF A	FF B	FF C	FF D
		A	B	C	D		A	B	C	D
1	0	1	1	1	1					
2	1	1	0	0	1					
3	1	1	1	1	1	↑				
4	1	1	1	1	1	↑				
5	1	1	1	1	1	↑				
6	0	1	1	1	1					
7	1	1	0	1	0					
8	1	1	1	1	1	↑				
9	1	0	1	1	1					
10	1	1	1	1	1	↑				
11	1	1	1	0	1					
12	1	1	1	1	1	↑				
13	1	1	1	1	1	↑				
14	0	1	1	1	1					
15	1	1	0	1	0					
16	1	1	1	1	1	↑				
17	1	1	1	1	1	↑				
18	1	1	1	0	1