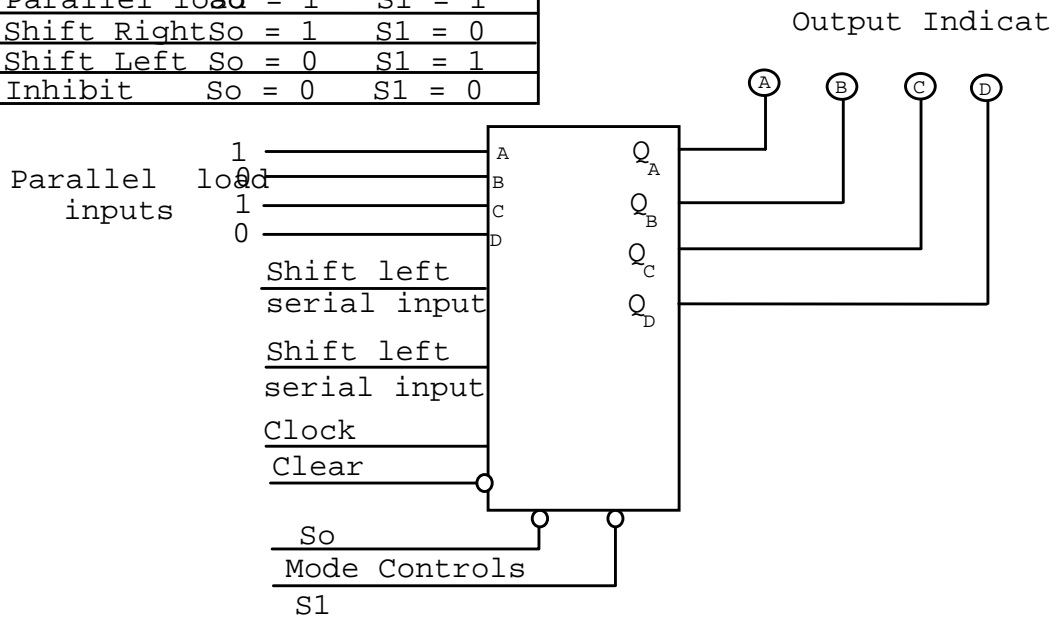


**Universal Shift Register (74194) In-Class Example**

Inputs							Outputs			
Line Number	Clear	Shift Left	Shift Right	S <sub>0</sub>	S <sub>1</sub>	Clock Pulse	A	B	C	D
1	0	X	X	X	X					
2	1	1	0	0	1	↑				
3	1	0	1	0	1	↑				
4	1	1	0	0	1	↑				
5	1	0	1	0	1	↑				
6	1	0	1	0	1	↑				
7	0	X	X	X	X					
8	1	0	1	1	0	↑				
9	1	1	0	1	0	↑				
10	1	0	1	1	0	↑				
11	1	0	1	1	0	↑				
12	1	0	1	1	0	↑				
13	1	1	1	1	1	↑				
14	1	1	0	0	1	↑				
15	1	0	1	1	0	↑				
16	1	1	0	1	0	↑				

Mode Control

Parallel load	S <sub>0</sub> = 1	S <sub>1</sub> = 1
Shift Right	S <sub>0</sub> = 1	S <sub>1</sub> = 0
Shift Left	S <sub>0</sub> = 0	S <sub>1</sub> = 1
Inhibit	S <sub>0</sub> = 0	S <sub>1</sub> = 0



### Universal Shift Register (74194) In-Class Example – Cont'd

Inputs							Outputs			
Line Number	Clear	Shift Left	Shift Right	S <sub>0</sub>	S <sub>1</sub>	Clock Pulse	A	B	C	D
1	0	X	X	X	X					
2	1	1	1	0	1	↑				
3	1	0	1	0	1	↑				
4	1	1	0	0	1	↑				
5	1	0	1	0	1	↑				
6	1	0	1	0	1	↑				
7	0	X	X	X	X					
8	1	0	1	1	0	↑				
9	1	1	1	1	0	↑				
10	1	0	0	1	0	↑				
11	1	0	0	1	0	↑				
12	1	0	1	1	0	↑				
13	1	1	0	1	1	↑				
14	1	1	0	0	1	↑				
15	1	0	1	1	0	↑				
16	1	1	0	1	0	↑				

Mode Control

Parallel load	S <sub>0</sub> = 1	S <sub>1</sub> = 1
Shift Right	S <sub>0</sub> = 1	S <sub>1</sub> = 0
Shift Left	S <sub>0</sub> = 0	S <sub>1</sub> = 1
Inhibit	S <sub>0</sub> = 0	S <sub>1</sub> = 0

