Lab #10 Name: _____ Per: _____

Title: D FLIP-FLOPS

Materials:
[1] 7474 D-type flip-flop IC
[1] clock (single pulses)

Procedure:

1. Insert the 7474 into the breadboard.
2. Refer to Figure 10 and wire the 7474.
3. Operate the *asynchronous* inputs CLR and PS according to the inputs in Table 10-1, and record the results in Table 10-1. Also write the name of the condition in the last column of the table. **Get Instructor's Signature.**
4. Disable the asynchronous inputs (PS and CLR to 1).
5. Operate the *synchronous* inputs D and CLK of the 7474 according to the inputs in Table 10-2. Observe and record the results in Table 10-2. **Get Instructor's Signature.**

Questions (answer on a separate piece of paper – **"Draw" means you must use a template**):

1. **Draw** a logic symbol for a D flip-flop. Label the inputs D, CLK, PS, and CLR and the outputs Q and $\overline{Q}$.
2. What are the synchronous inputs of the D flip-flop?
3. What are the asynchronous inputs of the D flip-flop?
4. Which output column in Table 10-2 is exactly the same as the input D column?
5. A logical _____ at PS will preset the Q output of the 7474 D flip-flop to a logical _____, assuming that CLR is a 1.
6. The synchronous inputs of the D flip-flop only operate when the PS and CLR inputs are _____ (disabled, enabled) with a logical _____.
7. The 7474 D flip-flop is a _____ (negative-, positive-) edge triggered flip-flop.
8. Explain why the D flip-flop is often referred to as the *delay* flip-flop.

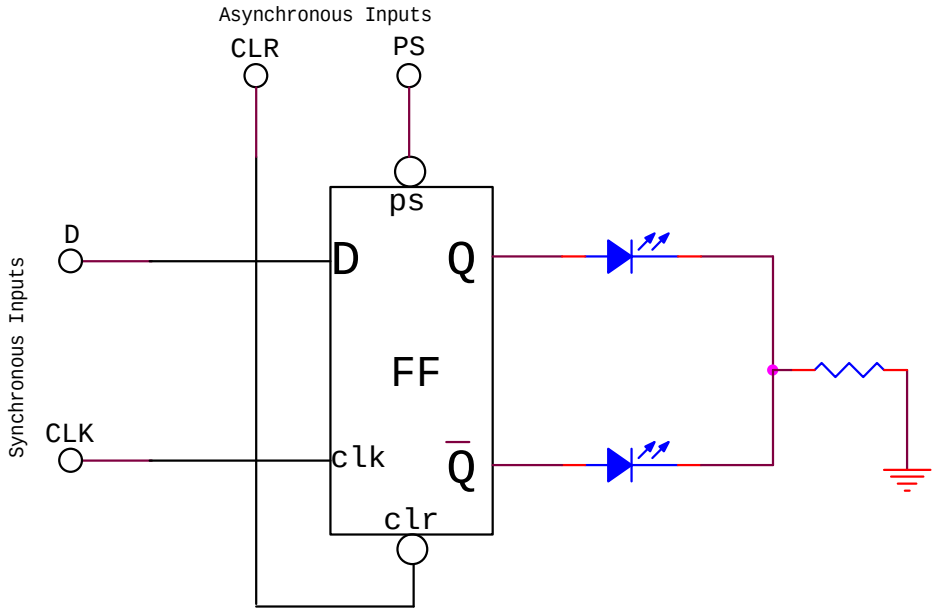

Figure 10 D-FlipFlop

Inputs		Outputs		
Preset	Clear	Q	$\overline{Q}$	Name of Condition
0	0			*Prohibited*
0	1			
1	0			
1	1			
				Clear Q to 0, Preset Q to 1, Disable asynchronous inputs

Table 10-1 TT for 7474 D Flip-Flop

(asynchronous inputs)

Inputs		Outputs			
Clock	Data	Before Clock Pulse		After Clock Pulse	
CLK	D	Q	$\overline{Q}$	Q	$\overline{Q}$
↑	0	0	1		
↑	0	1	0		
↑	1	0	1		
↑	1	1	0		

Table 10-2 TT for D Flip-Flop